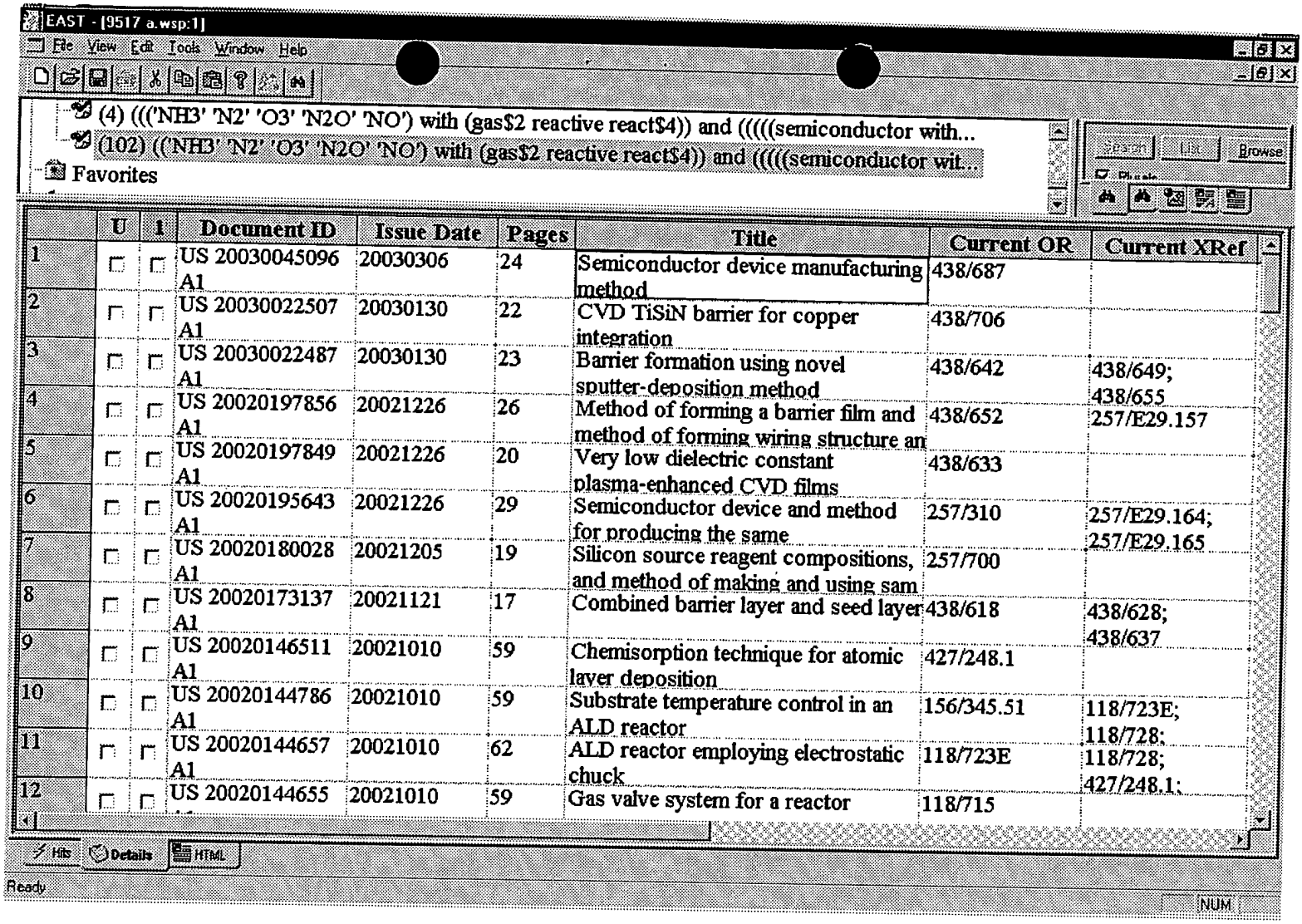
L Number	Hits	Search Text	DB	Time stamp
-	337714	semiconductor with substrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:34
-	13822	(semiconductor with substrate) and (silicon near3 source silicon adj containing si adj containing silicon adj material)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:37
-	13822	(semiconductor with substrate) and (silicon near3 source silicon adj containing si adj containing silicon adj material)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:35
-	337714	semiconductor with substrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:35
-	13822	((semiconductor with substrate) and (silicon near3 source silicon adj containing si adj containing silicon adj material)) and (semiconductor with substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:36
-	4226	(((semiconductor with substrate) and (silicon near3 source silicon adj containing si adj containing silicon adj material)) and (semiconductor with substrate)) and barrier	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:36
-	851	barrier with (silicon near3 source silicon adj containing si adj containing silicon adj material)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:38
-	396	barrier near5 (silicon near3 source silicon adj containing si adj containing silicon adj material)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:39
-	342525	('NH3' 'N2' 'O3' 'N2O' 'NO') with (gas$2 reactive react$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:42
-	851	(barrier with (silicon near3 source silicon adj containing si adj containing silicon adj material)) or (barrier near5 (silicon near3 source silicon adj containing si adj containing silicon adj material))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:43
-	452	((((semiconductor with substrate) and (silicon near3 source silicon adj containing si adj containing silicon adj material)) and (semiconductor with substrate)) and barrier) and ((barrier with (silicon near3 source silicon adj containing si adj containing silicon adj material)) or (barrier near5 (silicon near3 source silicon adj containing si adj containing silicon adj material)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:43

-	4	((('NH3' 'N2' 'O3' 'N2O' 'NO') with (gas$2 reactive react$4)) and (((((semiconductor with substrate) and (silicon near3 source silicon adj containing si adj containing silicon adj material)) and (semiconductor with substrate)) and barrier) and ((barrier with (silicon near3 source silicon adj containing si adj containing silicon adj material)) or (barrier near5 (silicon near3 source silicon adj containing si adj containing silicon adj material))))) and silazane	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 16:44
-	102	(('NH3' 'N2' 'O3' 'N2O' 'NO') with (gas$2 reactive react$4)) and (((((semiconductor with substrate) and (silicon near3 source silicon adj containing si adj containing silicon adj material)) and (semiconductor with substrate)) and barrier) and ((barrier with (silicon near3 source silicon adj containing si adj containing silicon adj material)) or (barrier near5 (silicon near3 source silicon adj containing si adj containing silicon adj material))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/04/01 17:13



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1	☐	☐	US 20030045096 A1	20030306	24	Semiconductor device manufacturing method	438/687	
2	☐	☐	US 20030022507 A1	20030130	22	CVD TiSiN barrier for copper integration	438/706	
3	☐	☐	US 20030022487 A1	20030130	23	Barrier formation using novel sputter-deposition method	438/642	438/649; 438/655
4	☐	☐	US 20020197856 A1	20021226	26	Method of forming a barrier film and method of forming wiring structure an	438/652	257/E29.157
5	☐	☐	US 20020197849 A1	20021226	20	Very low dielectric constant plasma-enhanced CVD films	438/633	
6	☐	☐	US 20020195643 A1	20021226	29	Semiconductor device and method for producing the same	257/310	257/E29.164; 257/E29.165
7	☐	☐	US 20020180028 A1	20021205	19	Silicon source reagent compositions, and method of making and using sam	257/700	
8	☐	☐	US 20020173137 A1	20021121	17	Combined barrier layer and seed layer	438/618	438/628; 438/637
9	☐	☐	US 20020146511 A1	20021010	59	Chemisorption technique for atomic layer deposition	427/248.1	
10	☐	☐	US 20020144786 A1	20021010	59	Substrate temperature control in an ALD reactor	156/345.51	118/723E; 118/728;
11	☐	☐	US 20020144657 A1	20021010	62	ALD reactor employing electrostatic chuck	118/723E	118/728; 427/248.1;
12	☐	☐	US 20020144655	20021010	59	Gas valve system for a reactor	118/715	

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13	☐	☐	US 20020142585 A1	20021003	21	Very low dielectric constant plasma-enhanced CVD films	438/633	
14	☐	☐	US 20020142538 A1	20021003	12	Process for fabricating RuSixOy-containing adhesion layers	438/238	
15	☐	☐	US 20020140890 A1	20021003	18	Liquid crystal display component and transparent conductive substrate suita	349/122	349/158
16	☐	☐	US 20020132374 A1	20020919	22	Method for controlling deposition of dielectric films	438/3	
17	☐	☐	US 20020125516 A1	20020912	12	RuSixOy-containing adhesion layers and process for fabricating the same	257/295	
18	☐	☐	US 20020096726 A1	20020725	11	Semiconductor device and manufacturing method thereof	257/384	
19	☐	☐	US 20020076881 A1	20020620	12	RuSixOy-containing adhesion layers and process for fabricating the same	438/250	
20	☐	☐	US 20020076508 A1	20020620	60	Varying conductance out of a process region to control gas flux in a	427/569	427/255.28; 427/377
21	☐	☐	US 20020076507 A1	20020620	59	Process sequence for atomic layer deposition	427/569	427/248.1
22	☐	☐	US 20020076490 A1	20020620	60	Variable gas conductance control for a process chamber	427/248.1	118/504; 118/715
23	☐	☐	US 20020076481 A1	20020620	59	Chamber pressure state-based control for a reactor	427/8	427/248.1
24	☐	☐	US 20020074577	20020620	12	RuSixOy-containing adhesion layers	257/250	

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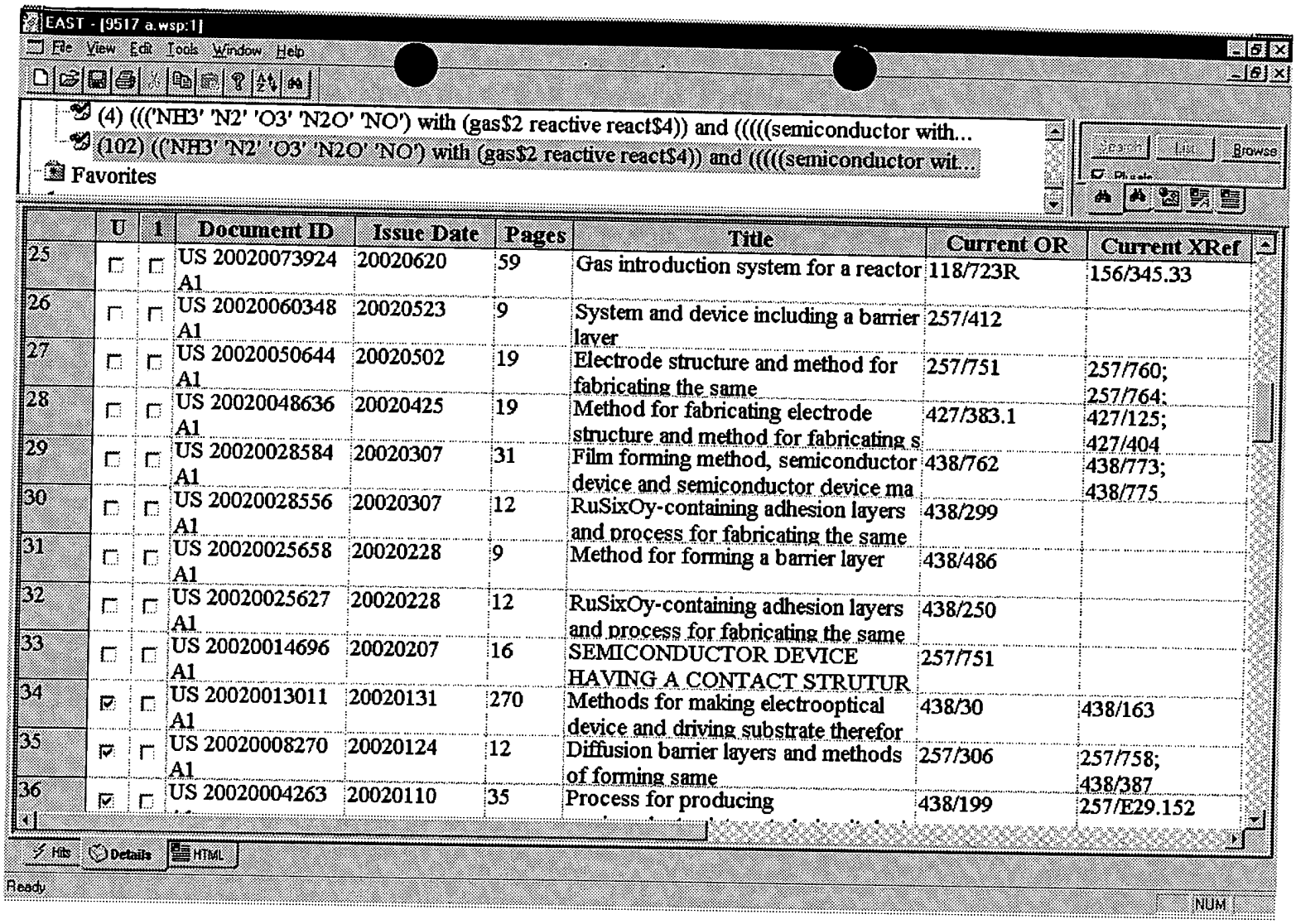

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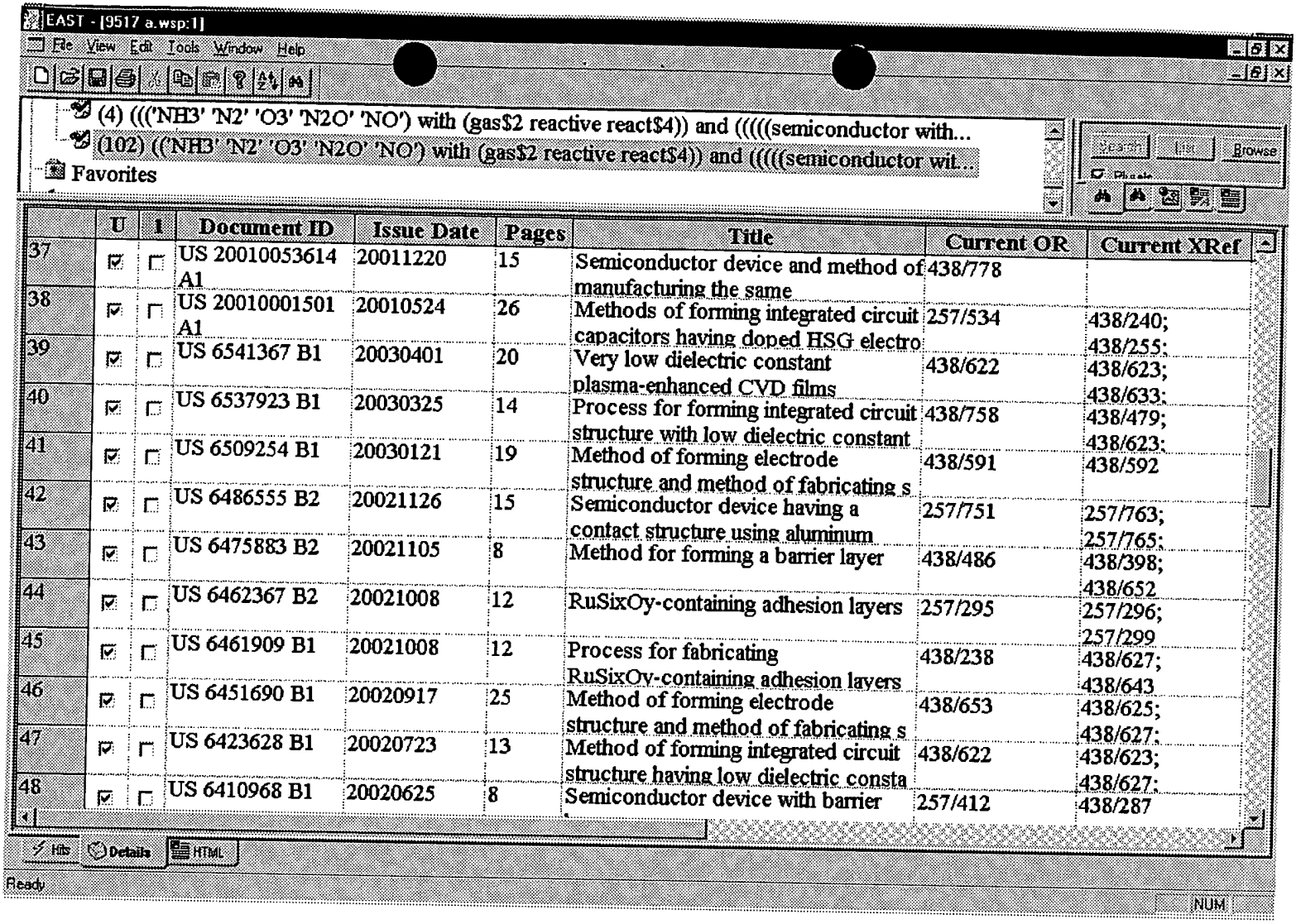
25	☐	☐	US 20020073924 A1	20020620	59	Gas introduction system for a reactor	118/723R	156/345.33
26	☐	☐	US 20020060348 A1	20020523	9	System and device including a barrier layer	257/412	
27	☐	☐	US 20020050644 A1	20020502	19	Electrode structure and method for fabricating the same	257/751	257/760; 257/764;
28	☐	☐	US 20020048636 A1	20020425	19	Method for fabricating electrode structure and method for fabricating s	427/383.1	427/125; 427/404
29	☐	☐	US 20020028584 A1	20020307	31	Film forming method, semiconductor device and semiconductor device ma	438/762	438/773; 438/775
30	☐	☐	US 20020028556 A1	20020307	12	RuSixOy-containing adhesion layers and process for fabricating the same	438/299	
31	☐	☐	US 20020025658 A1	20020228	9	Method for forming a barrier layer	438/486	
32	☐	☐	US 20020025627 A1	20020228	12	RuSixOy-containing adhesion layers and process for fabricating the same	438/250	
33	☐	☐	US 20020014696 A1	20020207	16	SEMICONDUCTOR DEVICE HAVING A CONTACT STRUTUR	257/751	
34	☑	☐	US 20020013011 A1	20020131	270	Methods for making electrooptical device and driving substrate therefor	438/30	438/163
35	☑	☐	US 20020008270 A1	20020124	12	Diffusion barrier layers and methods of forming same	257/306	257/758; 438/387
36	☑	☐	US 20020004263	20020110	35	Process for producing	438/199	257/E29.152



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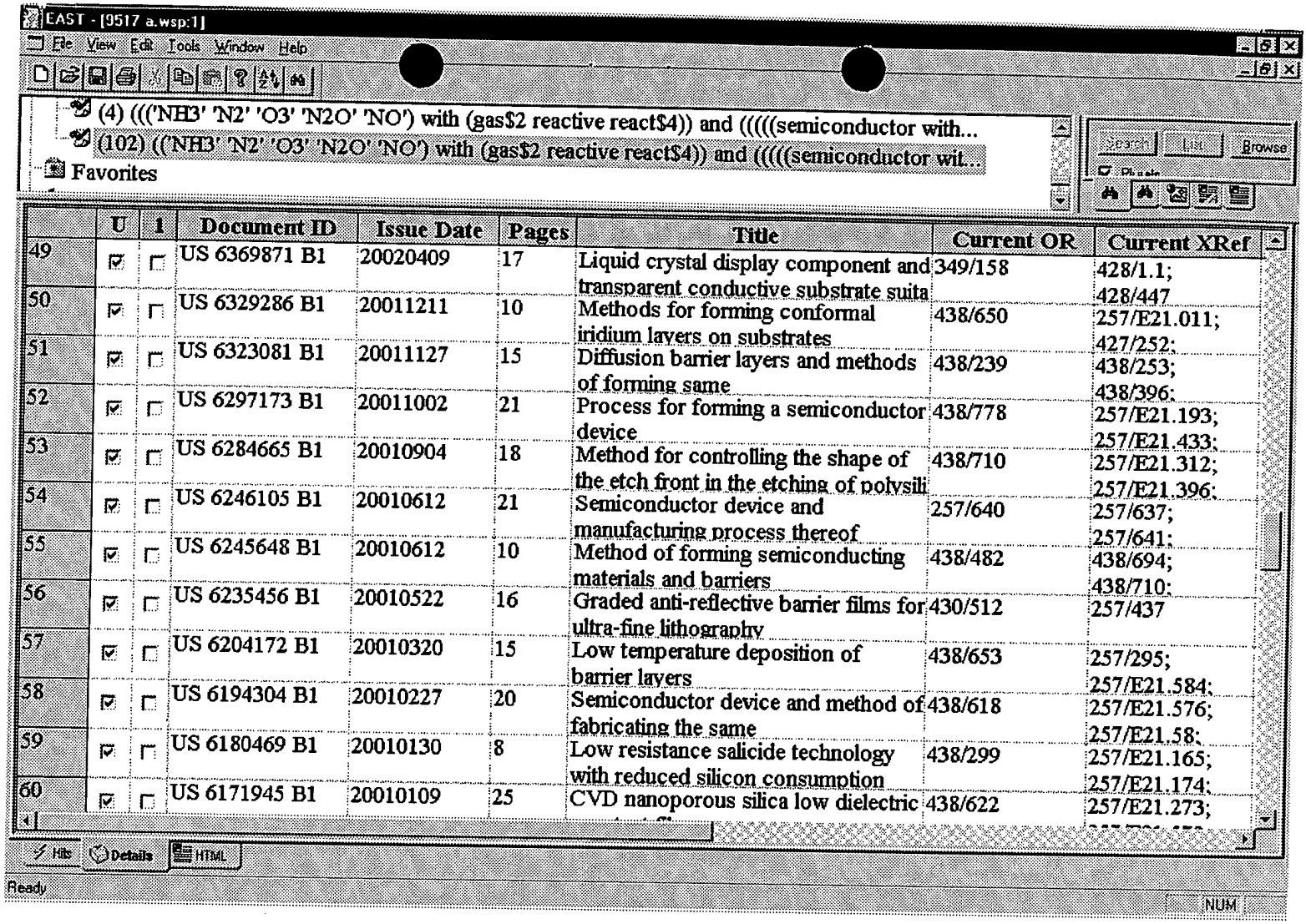
37	☑	☐	US 20010053614 A1	20011220	15	Semiconductor device and method of manufacturing the same	438/778	
38	☑	☐	US 20010001501 A1	20010524	26	Methods of forming integrated circuit capacitors having doped HSG electro	257/534	438/240; 438/255;
39	☑	☐	US 6541367 B1	20030401	20	Very low dielectric constant plasma-enhanced CVD films	438/622	438/623; 438/633;
40	☑	☐	US 6537923 B1	20030325	14	Process for forming integrated circuit structure with low dielectric constant	438/758	438/479; 438/623;
41	☑	☐	US 6509254 B1	20030121	19	Method of forming electrode structure and method of fabricating s	438/591	438/592
42	☑	☐	US 6486555 B2	20021126	15	Semiconductor device having a contact structure using aluminum	257/751	257/763; 257/765;
43	☑	☐	US 6475883 B2	20021105	8	Method for forming a barrier layer	438/486	438/398; 438/652
44	☑	☐	US 6462367 B2	20021008	12	RuSixOy-containing adhesion layers	257/295	257/296; 257/299
45	☑	☐	US 6461909 B1	20021008	12	Process for fabricating RuSixOy-containing adhesion layers	438/238	438/627; 438/643
46	☑	☐	US 6451690 B1	20020917	25	Method of forming electrode structure and method of fabricating s	438/653	438/625; 438/627;
47	☑	☐	US 6423628 B1	20020723	13	Method of forming integrated circuit structure having low dielectric consta	438/622	438/623; 438/627;
48	☑	☐	US 6410968 B1	20020625	8	Semiconductor device with barrier	257/412	438/287



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49	☑	☐	US 6369871 B1	20020409	17	Liquid crystal display component and transparent conductive substrate suita	349/158	428/1.1; 428/447
50	☑	☐	US 6329286 B1	20011211	10	Methods for forming conformal iridium layers on substrates	438/650	257/E21.011; 427/252;
51	☑	☐	US 6323081 B1	20011127	15	Diffusion barrier layers and methods of forming same	438/239	438/253; 438/396;
52	☑	☐	US 6297173 B1	20011002	21	Process for forming a semiconductor device	438/778	257/E21.193; 257/E21.433;
53	☑	☐	US 6284665 B1	20010904	18	Method for controlling the shape of the etch front in the etching of polysili	438/710	257/E21.312; 257/E21.396;
54	☑	☐	US 6246105 B1	20010612	21	Semiconductor device and manufacturing process thereof	257/640	257/637; 257/641;
55	☑	☐	US 6245648 B1	20010612	10	Method of forming semiconducting materials and barriers	438/482	438/694; 438/710;
56	☑	☐	US 6235456 B1	20010522	16	Graded anti-reflective barrier films for ultra-fine lithography	430/512	257/437
57	☑	☐	US 6204172 B1	20010320	15	Low temperature deposition of barrier layers	438/653	257/295; 257/E21.584;
58	☑	☐	US 6194304 B1	20010227	20	Semiconductor device and method of fabricating the same	438/618	257/E21.576; 257/E21.58;
59	☑	☐	US 6180469 B1	20010130	8	Low resistance salicide technology with reduced silicon consumption	438/299	257/E21.165; 257/E21.174;
60	☑	☐	US 6171945 B1	20010109	25	CVD nanoporous silica low dielectric	438/622	257/E21.273;

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61	☑	☐	US 6162744 A	20001219	10	Method of forming capacitors having high-K oxygen containing capacitor d	438/785	257/E21.008; 438/240;
62	☑	☐	US 6151347 A	20001121		Laser diode and method of fabrication thereof	372/45	372/96
63	☑	☐	US 6137176 A	20001024		Semiconductor device and method of fabricating the same	257/751	257/750; 257/752;
64	☑	☐	US 6107184 A	20000822		Nano-porous copolymer films having low dielectric constants	438/623	257/E21.259; 427/255.6;
65	☑	☐	US 6107182 A	20000822		Semiconductor device and method of fabricating the same	438/618	257/E21.165; 257/E21.576;
66	☑	☐	US 6103456 A	20000815		Prevention of photoresist poisoning from dielectric antireflective coating i	430/317	257/E21.029; 257/E21.257;
67	☑	☐	US 6074954 A	20000613		Process for control of the shape of the etch front in the etching of polysili	438/710	257/E21.312; 257/E21.396;
68	☑	☐	US 6069093 A	20000530		Process of forming metal films and multi layer structure	438/761	257/E21.165; 257/E21.17;
69	☑	☐	US 5972804 A	19991026		Process for forming a semiconductor device	438/786	257/E21.193; 257/E21.433;
70	☑	☐	US 5972765 A	19991026		Use of deuterated materials in semiconductor processing	438/308	257/E21.165; 257/E21.193;
71	☑	☐	US 5926734 A	19990720		Semiconductor structure having a titanium barrier layer	438/627	257/E21.584; 438/628;
72	☑	☐	US 5925494 A	19990720		Vapor deposition of polymer films	430/270.1	427/488;

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73	☑	☐	US 5874355 A	19990223		Method to prevent volcane effect in tungsten plug deposition	438/627	257/E21.584; 257/E21.585;
74	☑	☐	US 5837598 A	19981117		Diffusion barrier for polysilicon gate electrode of MOS device in integrate	438/532	257/E21.197; 257/E29.154;
75	☑	☐	US 5834804 A	19981110		Ferroelectric structure including MgTiO.sub.3 passivation	257/295	257/303; 257/632;
76	☑	☐	US 5695815 A	19971209		Metal carboxylate complexes for formation of metal-containing films o	427/226	257/E21.009; 257/E21.011;
77	☑	☐	US 5563102 A	19961008		Method of sealing integrated circuits	438/614	257/E23.167; 438/702;
78	☑	☐	US 5543634 A	19960806		Method of forming semiconductor materials and barriers	257/54	257/475; 257/55
79	☑	☐	US 5539551 A	19960723		LCD TFT drain and source electrodes having ohmic barrier, prim	349/42	257/59; 257/E27.111;
80	☑	☐	US 5472912 A	19951205		Method of making an integrated circuit structure by using a non-cond	438/643	257/E21.162; 257/E21.295;
81	☑	☐	US 5470784 A	19951128		Method of forming semiconducting materials and barriers using a multiple	438/61	118/719; 427/569;
82	☑	☐	US 5268590 A	19931207		CMOS device and process	257/764	257/371; 257/377;
83	☑	☐	US 5073804 A	19911217		Method of forming semiconductor materials and barriers	257/30	136/255; 136/258;
84	☑	☐	US 5064691 A	19911112		Gas phase borosiliconization of	427/252	148/279;

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85	☑	☐	US 5051812 A	19910924		Semiconductor device and method for manufacturing the same	257/758	257/761; 257/763;
86	☑	☐	US 5049523 A	19910917		Method of forming semiconducting materials and barriers	438/485	148/DIG.1; 438/92;
87	☑	☐	US 4968552 A	19901106		Versatile reactive ion etch barriers from polyamic acid salts	428/195	204/192.36; 216/62;
88	☑	☐	US 4902645 A	19900220		Method of selectively forming a silicon-containing metal layer	438/625	148/DIG.147; 148/DIG.19;
89	☑	☐	US 4760005 A	19880726		Amorphous silicon imaging members with barrier layers	430/65	430/57.5; 430/57.7;
90	☑	☐	US 4752815 A	19880621		Method of fabricating a Schottky barrier field effect transistor	257/346	257/471; 257/E29.271
91	☑	☐	US 4717637 A	19880105		Electrophotographic photosensitive member using microcrystalline silicon	430/65	430/66; 430/84
92	☑	☐	US 4681652 A	19870721		Manufacture of polycrystalline silicon	117/88	117/101; 117/102;
93	☑	☐	US 4678731 A	19870707		Electrophotographic photosensitive member having barrier layer comprisi	430/65	430/945
94	☑	☐	US 4587710 A	19860513		Method of fabricating a Schottky barrier field effect transistor	438/571	148/DIG.140; 257/280;
95	☑	☐	US 4470189 A	19840911		Process for making polycide structures	438/301	148/DIG.84; 204/192.32;
96	☑	☐	US 4430153 A	19840207		Method of forming an RIE etch	438/705	204/192.32;

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92	☑	☐	US 4681652 A	19870721		Manufacture of polycrystalline silicon	117/88	117/101; 117/102;
93	☑	☐	US 4678731 A	19870707		Electrophotographic photosensitive member having barrier layer comprisi	430/65	430/945
94	☑	☐	US 4587710 A	19860513		Method of fabricating a Schottky barrier field effect transistor	438/571	148/DIG.140; 257/280;
95	☑	☐	US 4470189 A	19840911		Process for making polycide structures	438/301	148/DIG.84; 204/192.32;
96	☑	☐	US 4430153 A	19840207		Method of forming an RIE etch barrier by in situ conversion of a silic	438/705	204/192.32; 257/E21.256;
97	☑	☐	US 4377031 A	19830322		Method of making Schottky barrier diode by selective beam-crystallized	438/487	117/904; 148/DIG.46;
98	☑	☐	US 4328258 A	19820504		Method of forming semiconducting materials and barriers	118/50.1	118/723E; 118/723VE;
99	☑	☐	US 4303467 A	19811201		Process and gas for treatment of semiconductor devices	438/720	204/192.32; 252/79.1;
100	☑	☐	US 4226897 A	19801007		Method of forming semiconducting materials and barriers	438/96	136/258; 204/164;
101	☑	☐	US 4214315 A	19800722		Method for fabricating vertical NPN and PNP structures and the resulting	257/517	257/516; 257/577;
102	☑	☐	EP 437307 A	19910717		High resistance poly:silicon load resistor - comprises structure includin		

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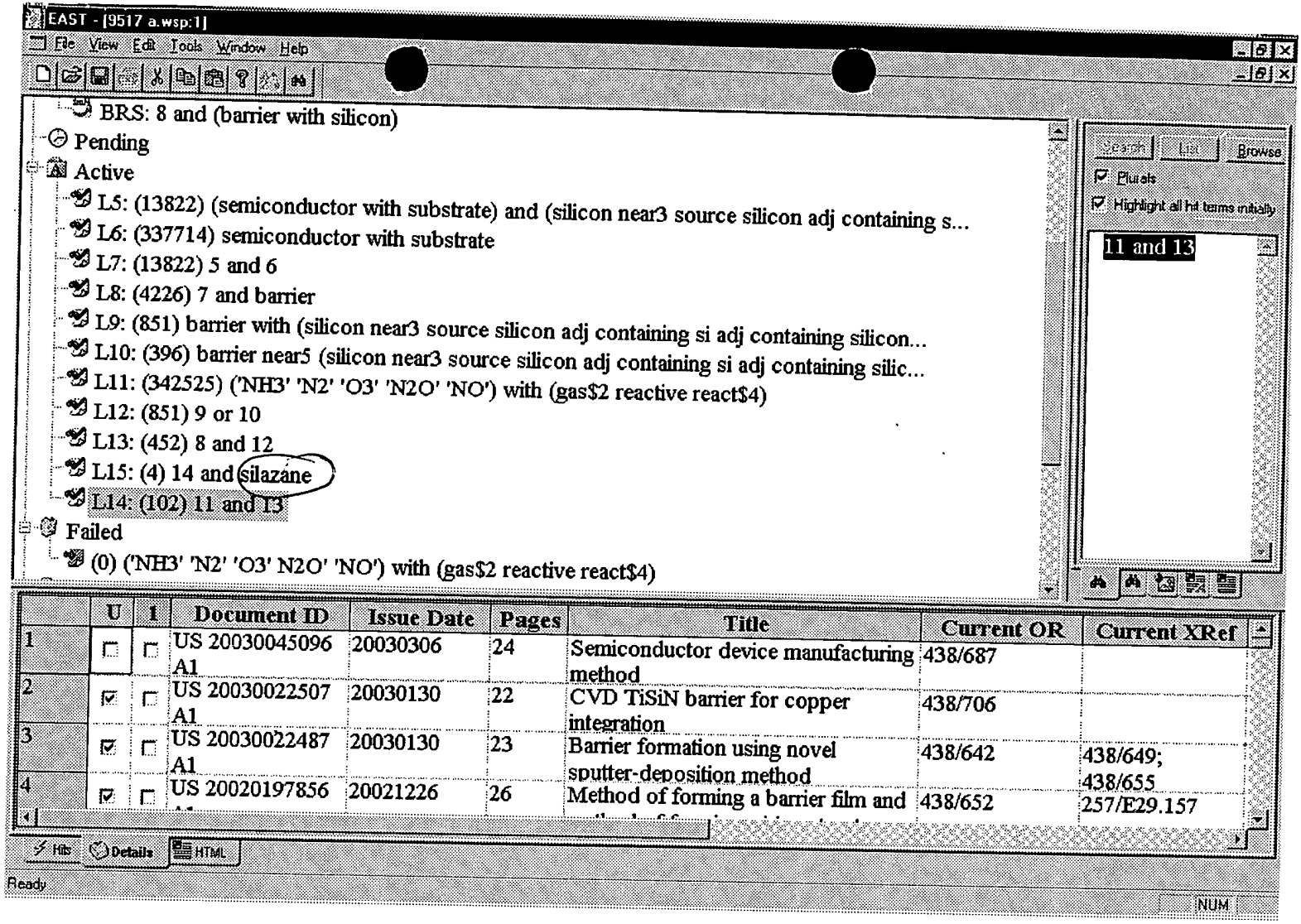

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1	☐	☐	US 20030045096 A1	20030306	24	Semiconductor device manufacturing method	438/687	
2	☑	☐	US 20030022507 A1	20030130	22	CVD TiSiN barrier for copper integration	438/706	
3	☑	☐	US 20030022487 A1	20030130	23	Barrier formation using novel sputter-deposition method	438/642	438/649; 438/655
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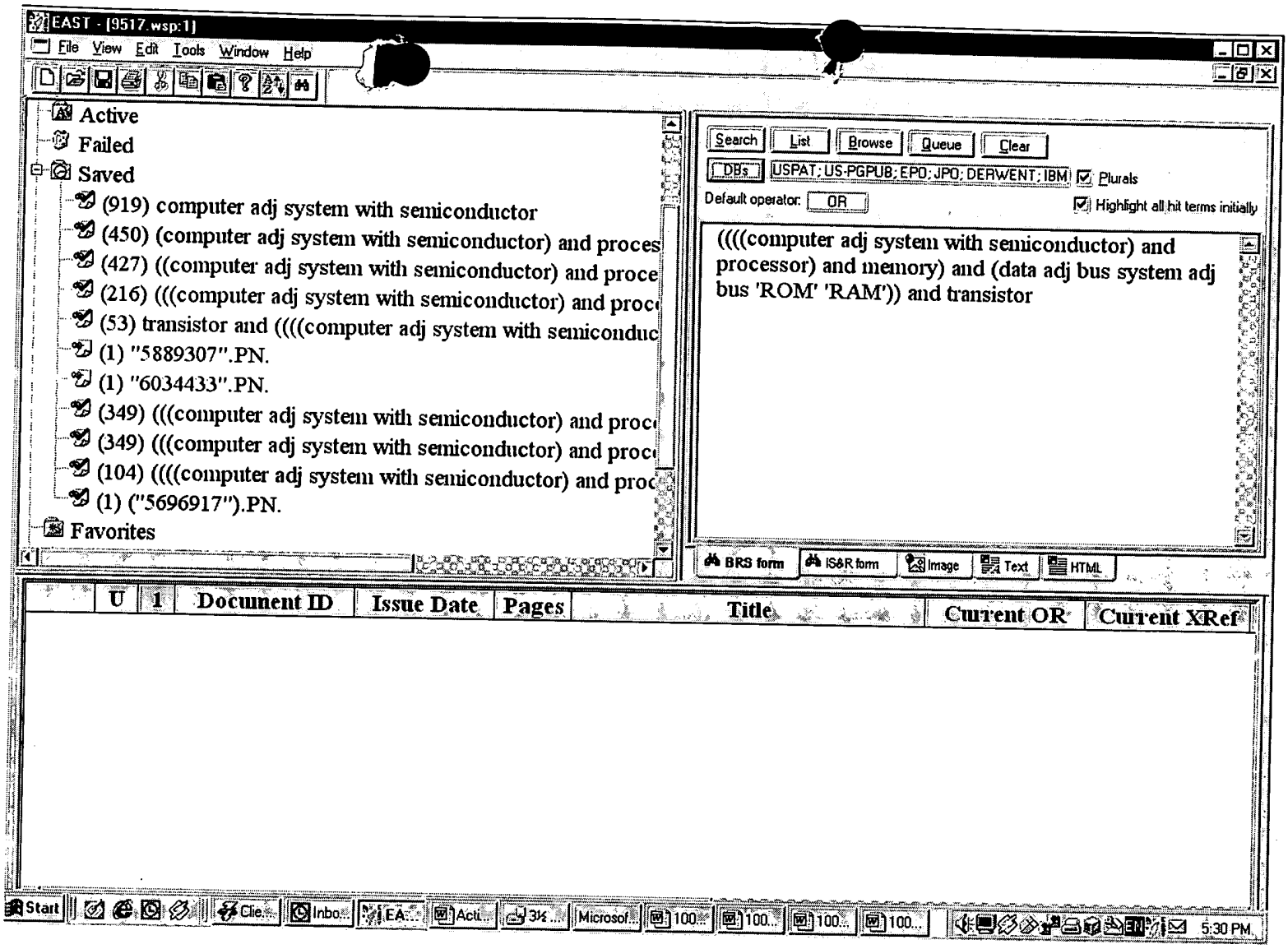
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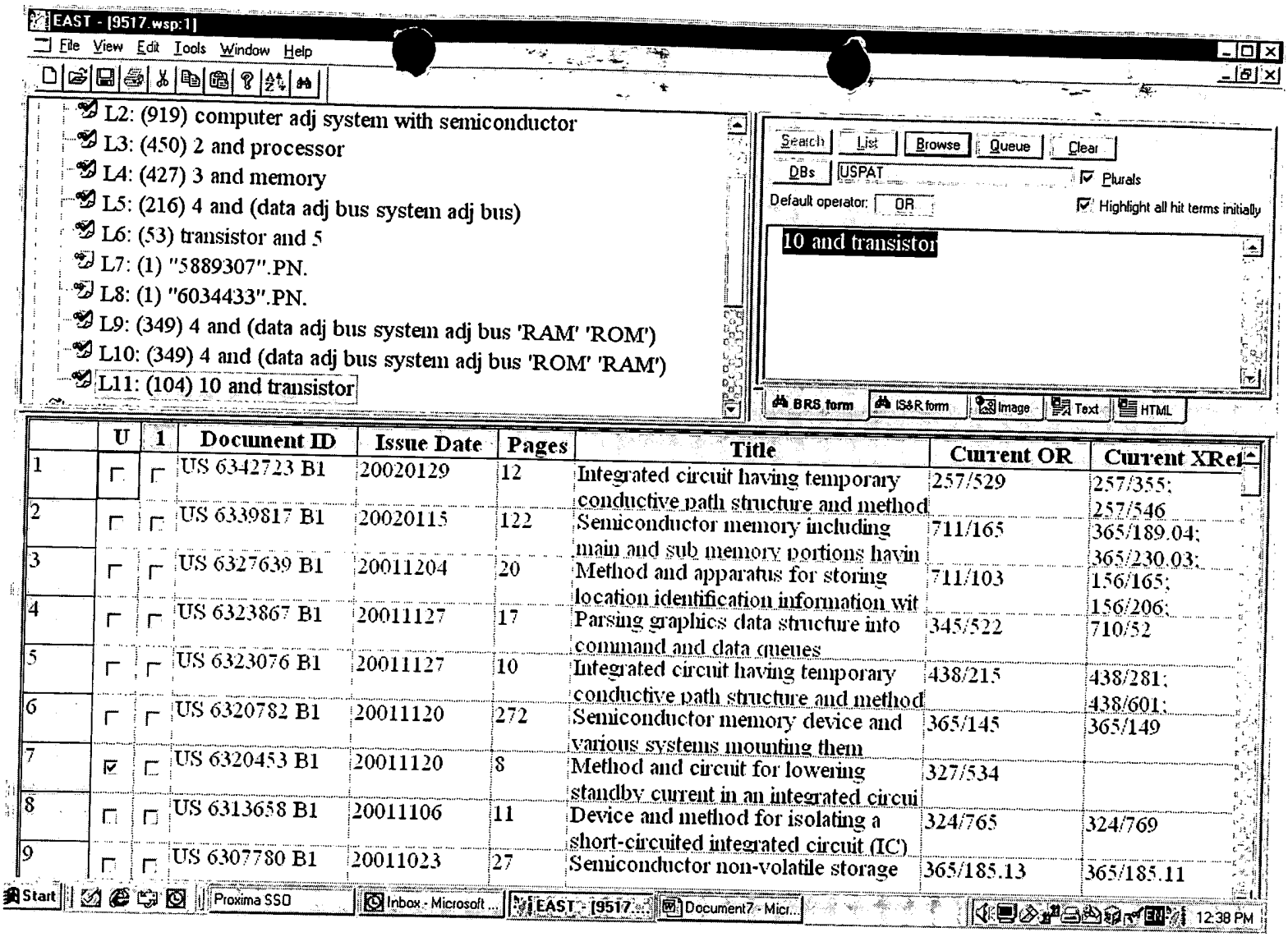
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L2: (919) computer adj system with semiconductor
L3: (450) 2 and processor
L4: (427) 3 and memory
L5: (216) 4 and (data adj bus system adj bus)
L6: (53) transistor and 5
L7: (1) "5889307".PN.
L8: (1) "6034433".PN.
L9: (349) 4 and (data adj bus system adj bus 'RAM' 'ROM')
L10: (349) 4 and (data adj bus system adj bus 'ROM' 'RAM')
L11: (104) 10 and transistor
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10 and transistor
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U 1 Document ID Issue Date Pages Title Current OR Current XRef
1 US 6342723 B1 20020129 12 Integrated circuit having temporary conductive path structure and method 257/529 257/355; 257/546
2 US 6339817 B1 20020115 122 Semiconductor memory including main and sub memory portions havin 711/165 365/189.04; 365/230.03;
3 US 6327639 B1 20011204 20 Method and apparatus for storing location identification information wit 711/103 156/165; 156/206;
4 US 6323867 B1 20011127 17 Parsing graphics data structure into command and data queues 345/522 710/52
5 US 6323076 B1 20011127 10 Integrated circuit having temporary conductive path structure and method 438/215 438/281; 438/601;
6 US 6320782 B1 20011120 272 Semiconductor memory device and various systems mounting them 365/145 365/149
7 US 6320453 B1 20011120 8 Method and circuit for lowering standby current in an integrated circui 327/534
8 US 6313658 B1 20011106 11 Device and method for isolating a short-circuited integrated circuit (IC) 324/765 324/769
9 US 6307780 B1 20011023 27 Semiconductor non-volatile storage 365/185.13 365/185.11
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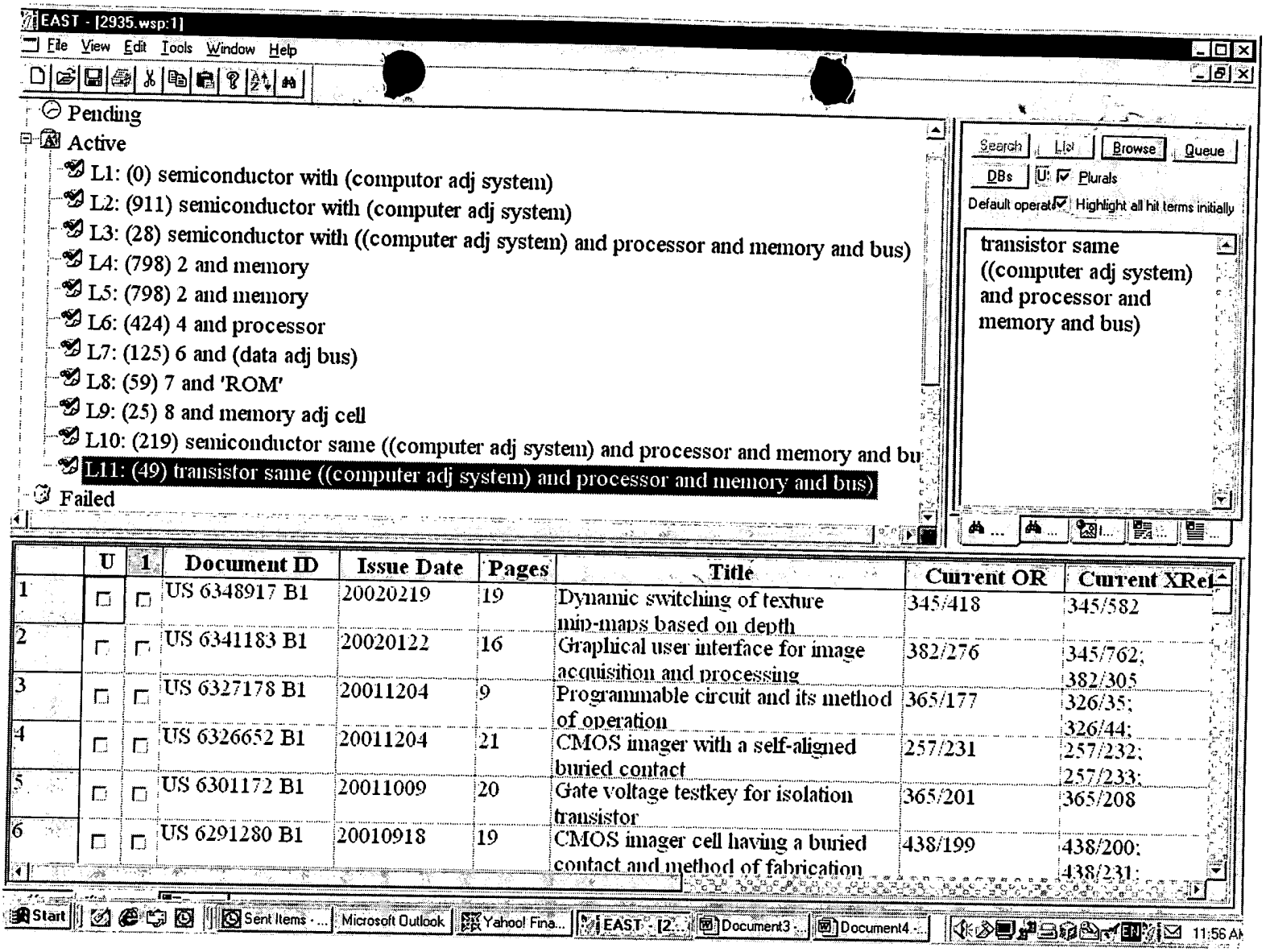

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6348917 B1	20020219	19	Dynamic switching of texture mip-maps based on depth	345/418	345/582
2	☐	☐	US 6341183 B1	20020122	16	Graphical user interface for image acquisition and processing	382/276	345/762; 382/305
3	☐	☐	US 6327178 B1	20011204	9	Programmable circuit and its method of operation	365/177	326/35; 326/44;
4	☐	☐	US 6326652 B1	20011204	21	CMOS imager with a self-aligned buried contact	257/231	257/232; 257/233;
5	☐	☐	US 6301172 B1	20011009	20	Gate voltage testkey for isolation transistor	365/201	365/208
6	☐	☐	US 6291280 B1	20010918	19	CMOS imager cell having a buried contact and method of fabrication	438/199	438/200; 438/231;